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Electrical Stability of Power Efficient Half Corbino Hydrogenated Amorphous Silicon Thin-Film Transistors

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In this paper, we study the electrical properties and current-temperature stress (CTS) induced electrical instability of half Corbino and fork-shaped hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) fabricated on the same substrate. The influence on overall electrical properties of the threshold voltage shift of half Corbino a-Si:H TFT is discussed in comparison to fork-shaped a-Si:H TFT. The results indicate that half Corbino a-Si:H TFT has improved ON-current levels and electrical stability in comparison to fork-shaped a-Si:H TFT with the similar structural dimension. © 2011 The Japan Society of Applied Physics

In order to achieve a high device width (W) to length (L) ratios in a limited layout space, interdigitated electrodes were first adapted in metal oxide semiconductor field-effect transistors (MOSFETs).[1,2] Organic thin-film transistors (OTFTs) also employed these structures to increase ON-current characteristics,[3,4] while bi-polar power transistors have generally used comb-like contact electrodes to minimize current crowding.[5] Recently, the comb-shaped electrodes have also been used in field-effect hydrogenated amorphous silicon (a-Si:H) solar cells to enhance the output power.[6] In a-Si:H TFT, one pair of interdigitated, so-called fork-shaped electrode was introduced to reduce a gate-to-source capacitance and a photo-leakage current that are critical for high-resolution active-matrix liquid crystal displays (AM-LCDs).[7,8]

Previously we reported the design and electrical properties of half-Corbino a-Si:H[9] and fork-shaped TFTs[10] to be used for active-matrix organic light-emitting diode (AM-OLED) displays. To assess potential of half-Corbino TFT for future display applications, it is essential to evaluate its electrical stability. In this paper, we report on the enhanced ON-current level of the fabricated half-Corbino a-Si:H TFT and its electrical stability in comparison to a conventional fork-shaped TFT fabricated using the same a-Si:H TFT technology. We present detailed studies of the current-temperature stress (CTS) induced electrical instability of half Corbino and fork-shaped a-Si:H TFTs.

Inverted stagger fork-shaped a-Si:H TFT and half Corbino a-Si:H TFT were fabricated with five photo-masks process used in the processing of the active-matrix liquid crystal displays (Fig. 1). Detailed process steps can be found in the previous publication.[9] As shown in Fig. 1(b), the fabricated half-Corbino a-Si:H TFT consists of rod-shape inner electrode (radius $R_1 = 5\,\mu m$) and half-circle shape outer electrode (radius $R_2 = 11\,\mu m$) while fork-shaped a-Si:H TFT [Fig. 1(a)] consists of rod-shape inner electrode (length $a = 6\,\mu m$) and U-shape outer electrode (overlap width $b = 10\,\mu m$). In both half Corbino and fork-shaped TFTs, the bottom gate electrode is large enough to cover entire channel region of transistor. In order to compare the output characteristics of half Corbino and fork-shaped a-Si:H TFTs for different drain bias conditions, we swept the drain bias from 0 to 20 V for a fixed gate bias (= 20 V) as in Fig. 2.

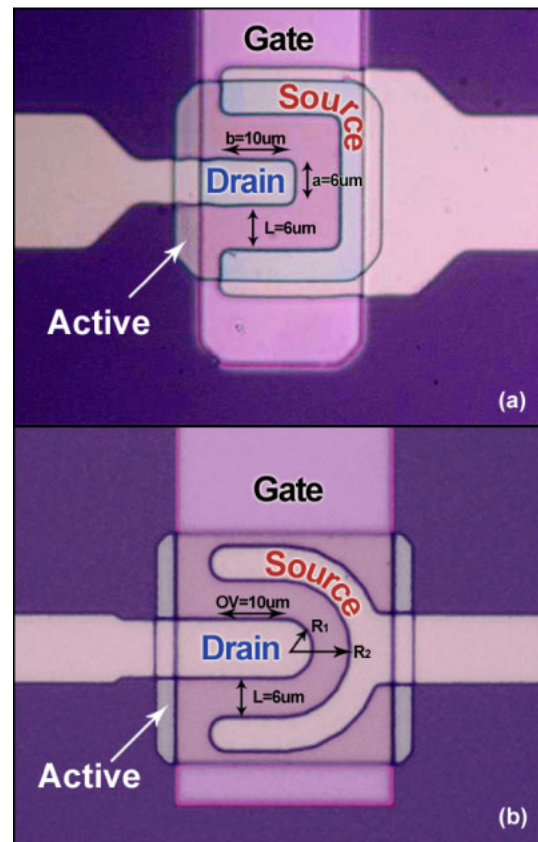

Fig. 1. (Color online) Photographs of the fabricated (a) fork-shaped and (b) half-Corbino a-Si:H TFTs. Drain to inner electrode and source to outer electrode.

Next, we measured the transfer characteristics of half-Corbino and fork-shaped a-Si:H TFTs; we swept the gate bias from 25 to 0 V and swept it again from 0 to 25 V for various drain voltages to extract their electrical parameters.

A series of CTS measurements of half Corbino and fork-shaped a-Si:H TFTs were performed by using a semiconductor parameter analyzer (HP 4156A) under an accelerated stress condition by setting the stress temperature (T_{STR}) at 80 °C. During the CTS measurements, we connected the gate and drain bias (inner-electrode) together and continuously applied the current through the drain to the TFTs. Source (outer-electrode) of the TFT was grounded. So the TFTs operate in the saturation regime. First, we applied same drain

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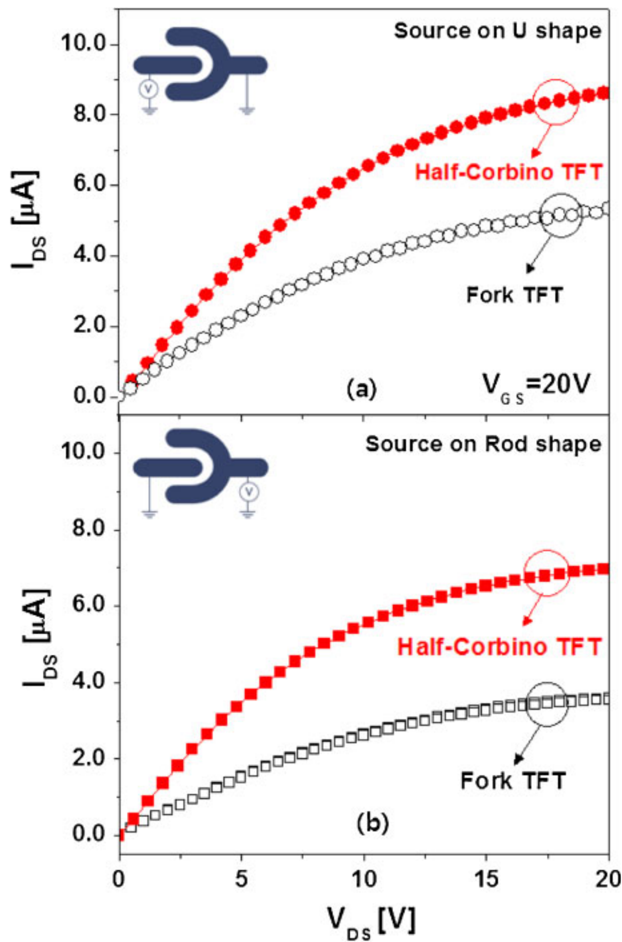

Fig. 2. (Color online) Comparison of output characteristics of half-Corbino and fork-shaped a-Si:H TFTs with the similar geometric dimension of channel length = 6 μm and overlap = 10 μm: where (a) source bias is on U-shape electrode, and (b) source bias is on rod shape electrode.

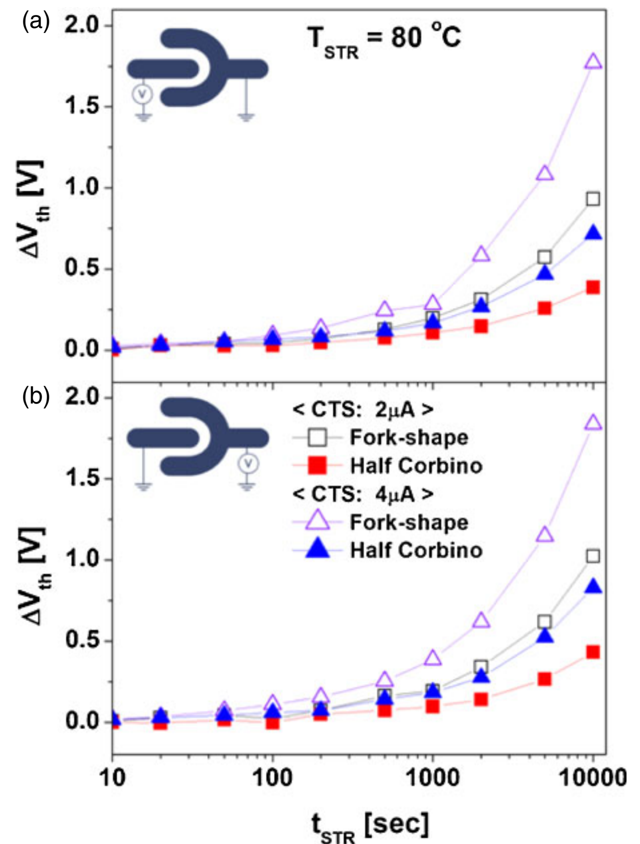

Fig. 3. (Color online) Threshold voltage shifts (ΔV_{th}) of half-Corbino and fork-shaped a-Si:H TFTs as a function of stress time (t_{STR}) in a semi-log scale for different drain bias conditions where (a) source bias is on U-shape electrode, and (b) source bias is on rod shape electrode. The applied current levels and the stress temperature (T_{STR}) are 2 μA, 4 μA, and 80 °C, respectively.

current values (I_{DS} = 2 and 4 μA) on U-shape electrode of each TFT that corresponds to the OLED luminance of 5,000 and 10,000 cd/m^2, respectively, for the emission efficiency of 3.0 cd/A and the pixel size of 300 × 100 μm^2.[10] The total stress time (t_{STR}) was 10,000 s, and we only interrupted the applied stress for 60 s to measure the transfer characteristics. We performed thermal annealing at 200 °C for 2 h to ensure the consistent initial properties of the a-Si:H TFTs before each CTS measurement.[11] Then, we changed the drain bias condition (drain current on rod shape electrode), and repeated the same CTS measurement for both TFTs. Using the effective channel width calculated by Lee *et al.*,[9,10] we extracted the threshold voltages using the maximum slope method over the stress time for each drain bias condition.[9] The threshold voltage shift (ΔV_{th}) is defined as follows: $\Delta V_{th}(t) = V_{th}(t = t_{STR}) - V_{th}(t = 0)$.

In order to calculate the power efficiency of half-Corbino TFT in comparison to fork-shaped TFT, we compare the output current levels of the fork-shaped TFT with half-Corbino TFT of the similar dimension as shown in Fig. 2. As shown in the figure, for the same drain bias voltage (= 20 V), the output current of half-Corbino TFT (= 8.64 μA) is larger than that of fork-shaped TFT with the similar dimension (= 5.33 μA) by 1.62 times. Even for the other bias condition (drain on the U-shape and source on the rod-shape electrode), half-Corbino TFT still shows a higher output current (= 6.99 μA) in comparison to fork-shaped TFT (= 3.61 μA). Since we already established previously that asymmetric electrode configuration results in the asymmetric electrical properties depending on the bias condition,[9,10] by using predefined geometric factors of half-Corbino and fork-shaped TFTs, the electrical parameters of each a-Si:H TFT are extracted and summarized for both bias conditions in Table I.

Table I. Extracted parameters of half Corbino TFT and fork-shaped TFT: (a) when source is applied on U-shaped electrode and (b) when source is applied on rod shaped electrode.

Bias condition	Source on rod shape		Source on U-shape	
	Fork-shaped	Half Corbino	Fork-shaped	Half Corbino
V_{TH} (V)	0.226	0.441	0.769	0.894
μ_{FE} (cm^2 V^{-1} s^{-1})	0.405	0.536	0.420	0.477
SS (mV/decade)	269.5	227.5	235.0	245.4

Figure 3 shows the ΔV_{th} results of half-Corbino TFT as a function of stress time (t_{STR}) in comparison to fork-shaped TFT. The ΔV_{th} of half-Corbino TFT for different stress currents (= 2 and 4 μA) on U-shape electrode are 0.39 and 0.72 V, respectively, while the ΔV_{th} of fork-shaped TFT for the same stress conditions are 0.93 and 1.77 V, respectively.

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When different stress currents are applied on the rod shape electrode, the ΔV_{th} of half-Corbino TFT are 0.43 and 0.83 V, respectively, while the ΔV_{th} of fork-shaped TFT are 1.02 and 1.84 V, respectively. ΔV_{th} increases with increasing stress current level for the same TFT structure. The increase of ΔV_{th} is larger in fork-shaped TFT than in half-Corbino TFT for the same stress current levels as well as for the same stress bias conditions! Because half-Corbino TFT exhibited smaller ΔV_{th} than fork-shaped TFT for all current stress conditions, half-Corbino TFT will have better electrical stability (less ΔV_{th}) compared to a fork-shaped TFT with the similar structure dimension. Field-effect mobility (μ_{eff}) was also extracted from the transfer characteristics. The amounts of μ_{eff} change ($\Delta\mu_{eff}$) after the CTS measurements are negligible from their initial values for both TFT structures.

The fork-shaped a-Si:H TFT is generally used in AM-LCD as a switching transistor due to its low gate-to-source capacitance (C_{GS}) and simple structure.[10] In comparison to fork-shaped TFT, we expect the half-Corbino TFT used as a switching TFT with source bias on the rod-type electrode will have an the enhanced switching time due to its higher ON-current level. In AM-OLED with a simple pixel circuit electrode including at least two transistors, the dynamic power consumption is expressed by following equation during the programming stage:

$$\mathrm{Power}_{\mathrm{program}} = fC_{\mathrm{Total}}V_{\mathrm{DS}}^2, \quad (1)$$

where f is the display driving frequency, and C_{Total} is sum of C_{GS}, C_{GD}, C_G, and C_{ST}. Here C_G is gate-to-channel capacitance, and C_{ST} is storage capacitance in AM-LCD. In general, the frame frequency and C_{ST} are fixed values in AMOLED. For half Corbino a-Si:H TFT, since the parasitic capacitance is reduced in comparison to standard TFT, the storage capacitor can be reduced to maintain the same feed-through voltage level resulting in a lower value of the total capacitance of switching TFT. Therefore, for a certain gray level (a fixed drain bias), the power consumption of each pixel can be linearly reduced resulting in better power efficiency and enhanced pixel aperture ratio due to the reduction of storage capacitor.

By changing the device bias condition where source bias is applied he U-shape electrode, ON-current of half-Corbino TFT can be increased. In this configuration, half-Corbino TFT can be also used as driving transistor for AM-OLED displays. During the driving state, the power consumption becomes a static model due to the DC bias (V_{DD}) on the driving transistor, and it is defined as the static power consumption ($\mathrm{Power}_{\mathrm{driving}}$) is expressed by following equation during the driving stage:

$$\mathrm{Power}_{\mathrm{driving}} = \frac{V_{\mathrm{DD}}^2}{R_{\mathrm{TFT}}}, \quad (2)$$

where R_{TFT} is the channel resistance determined by V_{GS} (gate node voltage defined at the programming stage). Therefore, in order to reduce the V_{DD} level, we need to use a transistor with a large channel width (W/L can be large). Considering that the channel length is usually fixed value in the current a-Si:H technology, the channel width needs to be increased to achieve the power reduction. Using half-Corbino geometry, we can achieve a larger W/L by about 1.6 times than fork-shaped TFT over the similar device area.[9]

In general, when the TFT is used as a driving transistor in AMOLED pixel circuit, it always suffers electrical stress by the OLED current since OLED is a current-driven device. Therefore, by using half-Corbino TFT as a driving TFT in the pixel circuit, we can expect a large enhancement in the electrical stability of pixel circuit for AMOLED due to the reduction of the effective channel width of transistor. This improvement in the electrical stability is achieved by the circle shape electrode of half-Corbino TFT which removes the sharp corners existing in fork-shaped TFT so that the locally intensified electric field in the channel can be alleviated to give a better device overall electrical performance and stability.[12]

In conclusion, we showed that due to the unique device geometry, the enhanced output current levels can be achieved in half-Corbino a-Si:H TFT under the same bias condition in comparison to fork-shaped a-Si:H TFT. We also studied the electrical instability of half-Corbino and fork-shaped TFTs under the current-temperature stress. It is found that the half-Corbino TFT shows better electrical stability compared to the fork-shaped TFT for similar W/L ratio despite of bias conditions. Enhanced electrical stability and improved output current properties of half-Corbino TFT are promising characteristics for the pixel circuit application in AM-OLEDs and other flat-panel displays.

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